AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A dual frame buffer system, comprising:

a first frame buffer;

a second frame buffer to store data used to refresh the display monitor; and

a controller to copy identified data updated within the first frame buffer to the second frame buffer and a display monitor when the identified data is needed to refresh the display monitor.

2. (Previously Presented) The dual frame buffer system claimed in claim 1, wherein the controller coordinates refresh of the display monitor using data stored in the second frame buffer and data updated within the first frame buffer.

3. (Original) The dual frame buffer system claimed in claim 1, further comprising:

a first address generator corresponding to the first frame buffer;

a second address generator corresponding to the second frame buffer; and

a timing generator for coordinating the timing between the first and second address generators for refreshing the display monitor.

4. (Previously Presented) The dual frame buffer system claimed in claim 3, further comprising:

a detector for detecting when an update is made to the data in the first frame buffer; and

a decoder for decoding the location of the updated data, wherein the controller to simultaneously transmit the updated data from the first frame buffer to the second frame buffer and the display monitor when the display monitor is refreshed.

5. (Original) The dual frame buffer system claimed in claim 4, wherein the first frame buffer comprises a plurality of regions.

6. (Previously Presented) The dual frame buffer claimed in claim 5, wherein the controller transmits those regions corresponding to the updated data from the first frame buffer to the second frame buffer and the display monitor when the display is refreshed.

7. (Original) The dual frame buffer claimed in claim 1, wherein the first frame buffer is part of a unified memory architecture.

8. (Original) The dual frame buffer claimed in claim 7, wherein the second frame buffer stores data used to refresh the display monitor.

9. (Previously Presented) A unified memory architecture system comprising:

a unified memory including a main memory and a primary frame buffer memory;

a secondary frame buffer memory; and

a controller to copy identified pixel data updated within the primary frame buffer memory to the secondary frame buffer memory and a display monitor when the identified pixel data is needed to refresh the display monitor.

10. (Previously Presented) The system claimed in claim 9, wherein the controller further coordinates refresh of the display monitor using pixel data stored in the second frame buffer and pixel data updated within the first frame buffer.

11. (Original) The system claimed in claim 10, further comprising:

a primary address generator corresponding to the primary frame buffer memory;

a secondary address generator corresponding to the secondary frame buffer memory; and

a timing generator for coordinating the timing between the primary and secondary address generators for refreshing the display monitor.

12. (Previously Presented) The system claimed in claim 11, further comprising:

a detector for detecting when an update is made to the pixel data in the primary frame buffer memory; and

a decoder for decoding the location of the updated pixel data, wherein the controller to simultaneously transmit the updated pixel data from the primary frame buffer memory to the secondary frame buffer memory and the display monitor when the display monitor is refreshed.

13. (Original) The system claimed in claim 12, wherein the primary frame buffer memory is partitioned into a plurality of regions.

14. (Previously Presented) The system claimed in claim 13, wherein the controller transmits those regions containing the updated pixel data from the primary frame buffer memory to the secondary frame buffer memory and the display monitor when the display monitor is refreshed.

15. (Previously Presented) A method of refreshing a display, comprising:

identifying data which is changed in a first frame buffer memory;

refreshing a display monitor using data contained within a second frame memory buffer; and

coordinating refreshing of the copying of the identified data from a first frame buffer memory to a second frame buffer memory and a display monitor when the identified data is needed to refresh the display monitor.

16. (Previously Presented) The method claimed in claim 15, further comprising:

transmitting the pixel data simultaneously from the first frame buffer memory to the second frame buffer memory and the display monitor.

17. (Previously Presented) The method claimed in claim 15, further comprising:

detecting when an update is made to the pixel data in the first frame buffer memory; and

decoding the location of the updated pixel data; and

transmitting the updated pixel data from the first frame buffer memory to the second frame buffer memory and the display monitor when the display monitor is refreshed.

18. (Original) The method claimed in claim 15, further comprising:

partitioning the first frame buffer memory into a plurality of regions.

19. (Previously Presented) The method claimed in claim 18, further comprising:

transmitting those regions containing the updated pixel data from the first frame buffer memory to the second frame buffer memory when the display is refreshed.

20. (Original) The method claimed in claim 15, wherein the first frame buffer memory is part of a uniform memory architecture memory.

21. (Previously Presented) A computer product for refreshing a display, comprising:

first computer readable program code embodied in a computer usable medium to cause a computer to identify data which is changed in a first frame buffer memory;

second computer readable program code embodied in a computer usable medium to cause a computer to refresh a display monitor using data contained within a second frame memory buffer; and

third computer readable program code embodied in a computer usable medium to cause a computer to coordinate refresh of the display monitor and copy of identified data from a first frame buffer memory to a second frame buffer memory and the display monitor when the data is changed in the first frame buffer memory and needed for refreshing the display.

22. (Previously Presented) The computer product claimed in claim 21, further comprising:

third computer readable program code embodied in a computer usable medium to cause a computer to transmit the pixel data simultaneously from the first frame buffer memory to the second frame buffer memory and the display monitor.

23. (Previously Presented) The computer product claimed in claim 21, further comprising:

third computer readable program code embodied in a computer medium to cause a computer to detect when an update is made to the pixel data in the first frame buffer memory; and

fourth computer readable program code in a computer usable medium to cause a computer to decode the location of the updated pixel data; and

fifth computer readable program code embodied in a computer usable medium to cause a computer to transmit the updated pixel data from the first frame buffer memory to the second frame buffer memory and the display monitor when the display monitor is refreshed.

24. (Original) The computer program claimed in claim 21, further comprising:

third computer readable program code embodied in a computer usable medium to cause a computer to partition the first frame buffer memory into a plurality of regions.

25. (Previously Presented) The computer produced claimed in claim 21, further comprising:

third computer readable program code embodied in a computer usable medium to cause a computer to transmit those regions containing the updated pixel data from the first frame buffer memory to the second frame buffer memory and the display monitor when the display monitor is refreshed.

26. (Previously Presented) A dual frame buffer system, comprising:

a first frame buffer;

a second frame buffer to store date used to refresh a display monitor; and

a controller to coordinate refresh of the display monitor using data stored in the second frame buffer and data updated within the first frame buffer.

27. (Previously Presented) The dual frame buffer system claimed in claim 26, further comprising:

a first address generator corresponding to the first frame buffer;

a second address generator corresponding to the second frame buffer; and

a timing generator to coordinate the timing between the first and second address generators for refreshing the display monitor.

28. (Previously Presented) The dual frame buffer system claimed in claim 27, wherein the first frame buffer comprises a plurality of regions.

29. (Previously Presented) The dual frame buffer system claimed in claim 27, further comprising:

a detector for detecting when an update is made to the data in the first frame buffer; and

a decoder for decoding the location of the updated data, wherein the controller to simultaneously transmit the updated data from the first frame buffer to the second frame buffer and the display monitor when the display monitor is refreshed.

30. (Previously Presented) The dual frame buffer claimed in claim 29, wherein the controller transmits those regions corresponding to the updated data from the first frame buffer to the second frame buffer and the display monitor when the display monitor is refreshed.